ASIC DESIGN ENGINEER RESUME

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Job Objective:

Looking for an ASIC Design Engineer position with company in which my past training and experiences can be used to help the business advance and meet goals.

Summary of Qualifications:

- Extensive experience in ASIC designing and programming
- Profound knowledge of signal processing circuit structure and architecture
- Steep knowledge of multi power domain designs, networking ASICs and Cadence IC CAD tools
- Solid understanding of ASIC design flow – logic design, verification, rtl coding, synthesis, timing and backend
- Proficient with MATLAB, CAD and C/C++
- Familiarity with FPGA emulation and IC testing
- Superior written and verbal communications skills

Work Experience:

ASIC Design Engineer, August 2005 – Present
MaxLinear, Inc, Boynton Beach, FL

- Evaluated system level design requirements and outlined top level chip schematics, pad definitions and floor-plan IC.
- Enforced schematic-level design and ensured verification of circuits.
- Formulated layout of critical circuits and analyzed specification compliance.
- Monitored problems and formulated solutions.
- Outlined design reviews at varied stages of design procedure.

ASIC Design Engineer, May 2000 – July 2005
MaxLinear, Inc, Boynton Beach, FL

- Offered leadership within the ASIC group and handled daily activities.
- Managed IC CAD tools and executed IC Layout.
- Arranged and attended design review meetings.
- Corresponded with foundries and vendors.
- Coordinated with project managers within the company.

Education:

Bachelor’s Degree in Electronics, Medaille College, Buffalo, NY

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Career Goal

Seeking the position of an ASIC Design Engineer to utilize my knowledge in ASIC, VLSI, SPI, RTL coding, CMOS digital and Verilog coding.

Technical Skills:

Vast competence to utilize cadence tools:

- ETS, QRC
- EDI, EPS, Orcad
- Conformal LEC

Adept with synopsys tools:

- Prime time, ICC

- Milkyway, Jupiter
- Formality, Astro

Thorough knowledge of programming languages:

- Perl, Python
- TCL, Verilog
- LEF/ DEF

Skilled at managing operating systems:

- Unix (Solaris)
- Linux- Red Hat
- Windows

Proficient in utilizing foundry chipsets:

- IBM 65nm and 90nm
- LSI 110nm
- TSMC low power 40nm

Familiarity with VLSI design tools:

- Magma Talus/ Blast fusion
- Mentor Calibre
- Cadence EDI

Talented in implementing programming languages:

- Java
- C, C++
- Cilk Plus

Sound capabilities to:

- Interpret CPU architectures and basic components
- Execute networking protocols and standards

Relevant Experience:

ASIC Design Engineer — January 2012 – Present
Nvidia Corporation — Washington, DC

- Provided assistance for designing services of micro and peripheral controllers.
- Assisted teams of architects and design engineers for development of ASIC applications.
- Implemented procedures for synthesis, timing, RTL designing and silicon setting of systems.
- Executed processes for development of micro-architecture solutions as per relevant specifications.
- Integrated designing IP services into business units relating to Broadband applications.
- Debugged customer issues, test cases, designing and system implementation issues.
- Resolved network processor blocks and problems by developing test benches at unit levels.
- Supported team members to monitor operations by preparing checkers and coverage services in system Verilog.

ASIC Design Engineer — November 2010 – January 2012
OmniVision Technologies — Santa Clara, CA

- Monitored existing critical silicon technologies as per customer product needs.
- Conducted demonstrations of Intel processes for external customer by critical designing and methodology evaluation.
- Assisted in designing and development of ASIC designs for RTL applications, related logic, timing and extraction.
- Provided assistance for efficient designing methodology through usage of standard automation tools.
- Performed designing and verification services for various interface and IP applications.
- Prepared detailed tests plans, block and system test benches, verification domain and formal test cases.
- Suggested procedures for convergence of timing, power and layout for various system designs.
- Developed test benches, test cases, reference models for various emulation and validation system technologies.

Educational Background:

Bachelor's Degree in Electrical Engineering — August 2006 – May 2010
Moraine Park Technical College — Fond du Lac, WI