DESIGN VERIFICATION ENGINEER RESUME

Objective:

Searching for an opportunity to maximize my skills as a Design Verification Engineer with well-organized and growing company.

Summary of Skills:

- Vast experience with Verilog Test Bench development and
- Outstanding knowledge of verification language
- Sound knowledge of ASIC verification, ASIC RTL design and RTL verification
- Familiarity with Verilog/C/C++ testbenches and verification environments
- Ability to work on various Vera programming skills
- Ability to communicate in both written and oral forms
- Skilled to prepare computer architecture
- Excellent programming and scripting skills

Professional Experience:

Design Verification Engineer, August 2005 – Present
A Technology Company, Middlebourne, WV

- Developed test plans and ensured that it covered first working silicon for processes.
- Designed function models of processes and validated architecture for it.
- Ensured that schedule for test plan was followed.
- Coordinated with logic designer and resolved all bugs in systems and assisted software developers in product development.
- Trained new engineers in verification flows.
- Developed various shell scripts for infrastructure.

Design Verification Engineer, May 2000 – July 2005
Apple, Middlebourne, WV

- Designed test cases and debugged systems.
- Documented all verification process carried on systems and tracked their progress.
- Performed debug and provided gate level simulation to systems.
- Provided support to silicon projects.
- Developed various software tools such as tools to provide test coverage.
- Ensured projects compliance with its interfaces and evaluated circuit faults.

Education:

Bachelor’s Degree in Computer Engineering, Centenary College, Hackettstown, NJ

Master’s Degree in Computer Engineering, New Jersey City University, Jersey City, NJ