# DFT ENGINEER RESUME

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## Career Goal:

Seeking the position of a DFT Engineer in your prestigious organization to be able to share my skills in BSEE, DFT, C, C++, VLSI, Perl, TCL, RTL coding and Unix shell scripts.

## Technical Skills:

Sound technical knowledge of Design tools including:

- Spectre, Synopsis, Matlab
- TetraMax, Xilinx, ModelSim
- Cadence- Virtuoso

Adept in utilizing programming languages:

- Verilog, C, C++
- OVM
- System Verilog

Thorough with hardware configuration:

- Schematic and layout design
- Full and semi -custom block design
- DFT techniques

Operating system expertise:

- FreeBSD
- MS Windows
- Mac OS, Linux

Adroit in handling Synopsys tools like:

- Design Compiler
- DFT Compiler, DFT Max
- DC- Topographical

Superb in deploying Cadence applications:

- IP Model Packager
- NCSim

High expertise in implementing testing tools:

- Function Generator
- Logic Analyzer
- Oscilloscope

Strong capabilities to:

- Comprehend DFD methodology to test high performance processors
- Formulate technical writing and maintain documentation

## Relevant Experience:

DFT Engineer
Smartplay Technologies
January 2012 – Present
Stockton, CA

- Collaborated with team to catalogue DMT specifications.
- Administered DFT implementations and effectuated DFT architecture and ECOs.
- Worked with test engineers to perform debug of silicon issues.
- Performed and evaluated DFT-centric modules using at-speed scan and JTAG.
- Performed scan insertion, silicon validation and functional test fault grading.
- Formulated test vector patterns, analyzed and resolved coverage issues.
- Supported designers to troubleshot STA, power and logical issues.

- Provided training to junior DFT engineers on DFT practice, theory and education.

DFT Engineer
Innovative Logic Inc.
November 2010 – January 2012
San Jose, CA

- Assisted in implementing DFT RTL design, DFT insertion and verification, MBIST insertion, coverage and static timing analysis.
- Cooperated with design team to devise and use test modes for ASIC.
- Consulted design team to ensure DFT design meets relevant standards.
- Assisted in devising, improving and managing test scripts.
- Worked with design team on IDDQ constrain validation and IVA analysis.
- Performed replication and analysis of ATPG and MBIST patterns.
- Applied MBIST, JTAG circuitry to produce repeatable signatures.
- Collaborated with engineering teams to design test scripts for identifying and resolving ATE issues.

## Educational Background:

Bachelor's Degree in Electronic Engineering
Nicolet Area Technical College
August 2006 – May 2010
Rhinelander, WI