IC LAYOUT DESIGNER RESUME

Objective:

To take a challenging role as an IC Layout Designer in a highly technical company where I could utilize my skills in Opus Layout design software and other verification tools and use these skills in providing quality service to the company.

Education:

Master in Computer Applications, 2002 Yale University

BS In Electronics, 1999 Yale University

Skills:

- Expert in Cadence Opus layout design software
- UNIX and Sun OS
- Verification Tools: DRC-LVS, Cypress rule checks, CLDRC and STRESS
- MS Tools: Word, Outlook, Excel
- · Strong Analytical skills
- Analog concepts such centroid matching, interdigitating

Professional Experience:

- Senior IC Layout Designer, 2008-present
- · Halex Corp., Georgetown, MA

Responsibilities:

- Performed tests on analog layout circuits for demod block for radio and USB circuits.
- Implemented the use of EDA tools such as Virtuoso Layout editor in performing feasibility studies.
- Developed multiple cell libraries for phase picker, op-amps and transistors.
- Analyzed the flow of common centroid matching and interdigitating of transistors.
- Intergraph Layout Designer, 2005-2008
- · Halex Corp., Georgetown, MA

Responsibilities:

- Developed full part-custom and full custom analog layouts.
- Collaborated with a team of analog experts in mitigating the effects of etching and doping to dummy devices.
- Planned and organized semiconductor analog layouts for various devices.
- Performed lay outing for full analog custom compressor system.
- IC Layout Designer, 2002-2005
- · Halex Corp., Georgetown, MA

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Certifications and Affiliations:

Certificate in Virtuso Layout editor Association of Layout Designers in Georgetown

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