MASK LAYOUT DESIGNER RESUME

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Career Goal:

To join your esteemed organization as Mask Layout Designer and enhance organization effectiveness owing to my skills in DRC, mark design, Cadence, CMOS digital and Calibre.

Technical Skills:

High technical knowledge of Layout tools like:

- Tanner Layout Editor
- Cadence Virtuoso Layout Editor
- PCell utility

Thorough with multiple platforms:

- Unix
- Linux
- Windows

Proficient with programming languages:

- C, Perl
- VHDL
- MVS, VMS

Solid understanding of synopsys including:

- Apollo
- Milkyway
- Astro, Hercules

Technically sound with layout designs including:

- CMOS digital
- SRAM IP

Through with IDE's:

- C Compiler
- Linker
- Assembler

Crystal clear with design concepts:

- Matching and shielding techniques
- Floor planning
- Layout design integration

Immense capabilities to:

- Create effective mask designs of embedded SRAM
- Utilize standard CMOS practices

Relevant Experience:

Mask Layout Designer
Cypress Semiconductor Corporation
January 2012 – Present
Anaheim, CA

- Developed layout designs for assigned projects as per design specifications.
- Communicated design status reports to engineering team members in accurate and concise manner.
- Provided technical assistance for enhancements of advanced tools, techniques and procedures.
- Suggested appropriate layout methodology for chips as per electrical, performance, reliability and schedule issues.
- Performed checking and verification of all procedures and checks in correct way.
- Coordinated with design engineering teams for planning and development of layout strategies.
- Assisted in layout and components for various circuit connections through advanced functions of CAD tools.

- Monitored mask design engineers activities such as floor plans and layouts.

Mask Layout Designer
Intel Corporation
November 2010 – January 2012
Hillsboro, OR

- Coordinated with engineering teams for preparation of new devices for protection of circuits.
- Provided technical assistance for efficient implementation of testing and debugging software packages.
- Developed Poly Fill Projects for reduction of cavity and stabilization of processes in automated manner.
- Performed protection measures of chip from static discharge functions by maintenance of Pad and TSV designs.
- Assisted in development of mask layouts for various types of VLSI circuits and support activities.
- Implemented procedures and multiple functions for DRAM research and development functions.
- Designed programs and layouts for areas such as speed, area, manufacturing yield and reliability.
- Executed software designs and package productivity software through Perl, TCL and scripting languages.

Educational Background:

Bachelor's Degree in Computer Engineering
Santa Barbara City College
August 2006 – May 2010
Santa Barbara, CA