RTL ENGINEER RESUME

Milford Newman
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Career Goal:

To be able to contribute to Company's growth and development as a RTL Engineer and share my expertise in RTL design, STA, Ethernet PCS, Perl scripting and Verilog.

Technical Skills:

Profound knowledge of RTL designing involving:

- Verilog/ VHDL design
- Area/ timing/ power evaluation
- Coding technical specifications

Adept in utilizing EDA tools like:

- Xilinx ISE
- Altera Quartus
- Aldec/ Riviera

Vast potential to implement software solutions using:

- C, Perl, uBoot
- Unix, Linux
- Windows, MS Office

Solid understanding of application of RF skills:

- Diplexer
- Transceivers, Noise Figure
- Non linearity effects

Strong knowledge of hardware description languages like:

- Verilog/ VHDL Matlab
- Simulink
- Perl TCL Specman

Digital skills specialization:

- Board Bringup
- Altera/ Xilinx FPGA Platforms
- Power supply design

Expertise in HDLs and HVLs utilization:

- Verilog A
- VHDL, Specman
- Vera

Immense capabilities to:

- Create VLSI circuit designs
- Complete RTL coding and verification

Relevant Experience:

RTL Engineer
Cadence Design Systems
January 2012 – Present
La Puente, CA

- Resolved RT related issues in collaboration with team of engineers and software developers.
- Provided automation of integrating SoC solutions, Hard Macro and Peripherals.
- Supported implementation of logic components by designing and development of Architecture and related specifications.
- Provided appropriate technical guidance regarding designing of microprocessor and electronic components.
- Maintained documentation of RTL flow processes such as simulations and archiving.

- Supported product release process by proper testing such as validation, regression, sensitivity and field tests.
- Performed review functions of board schematics and layouts for new engineering designs and platforms.
- Developed cell libraries and functional units by providing logic designs and simulation techniques.

RTL Engineer
Schweitzer Engineering Laboratories, Inc.
November 2010 – January 2012
Seattle, WA

- Resolved problems in RF and relevant hardware system by designing workarounds.
- Supported functional validation and power margin issues in collaboration with validation teams.
- Assisted in development and refinement of RTL engineering designs to meet performance goals.
- Provided assistance in designing and development of new RF applications to support frequency bands.
- Conducted reviews of board schematics and layouts for new RTL designs and platforms.
- Assisted in achievement of targets for modulation rates, bandwidths and RF frequency bands.
- Implemented data validation and debugging of RF applications to support relevant frequency bands.
- Maintained system documentation for RTL work flow procedures such as simulation and archiving.

Education Summary:

Bachelor's Degree in Electrical Engineering
Chippewa Valley Technical College
August 2006 – May 2010
Eau Claire, WI

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